DYNAMIC RANDOM ACCESS MEMORY DEVICES AND METHOD OF CONTROLLING REFRESH OPERATION THEREOF

ABSTRACT

A Dynamic Random Access Memory (DRAM) device can include a DRAM cell array configured to be periodically refreshed and a refresh control circuit that is configured to issue an internal refresh command to the DRAM cell array to provide periodic refresh of the DRAM cell array. The refresh control circuit can further include a refresh information signal to external of the DRAM device before the internal refresh command is issued to the DRAM cell array.